IN THE SPECIFICATION:

Please replace paragraph number **[0002]** with the following rewritten paragraph:

**[0002]** Field of the Invention: The present invention relates to a method for forming an interconnection for receiving bumps or balls of a semiconductor device for testing or burn-in of the device. In particular, the present invention relates to a method for forming ~~sloped-wall~~ sloped-wall, metal-lined interconnections to receive and contain portions of solder balls of a semiconductor device therein.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

**[0005]** Bare semiconductor dice are usually tested at least for continuity, and often more extensively, during the semiconductor die fabrication process and before packaging. Such more extensive testing may be, and has been, accomplished by placing a bare semiconductor die in a temporary package having terminals aligned with the terminals (bond pads) of the semiconductor die to provide electrical access to the circuits on the semiconductor die and subjecting the semiconductor die via the assembled temporary package to burn-in and discrete testing. Such temporary packages may also be used to test entire semiconductor wafers prior to singulating the semiconductor wafers into individual semiconductor dice. Exemplary ~~state-of-the-art~~ state-of-the-art fixtures and temporary packages for semiconductor die testing are disclosed in U.S. Patents 5,367,253; 5,519,332; 5,448,165; 5,475,317; 5,468,157; 5,468,158; 5,483,174; 5,451,165; 5,479,105; 5,088,190; and 5,073,117. U.S. Patents 5,367,253 and 5,519,332, assigned to the assignee of the present application, are each hereby incorporated herein for all purposes by this reference.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

**[0006]** Discrete testing includes testing the semiconductor dice for speed and for errors which may occur after fabrication and after burn-in. Burn-in is a reliability test of a semiconductor die to identify physical and electrical defects which would cause the semiconductor die to fail to perform to specifications or to fail altogether before its normal operational life cycle is reached. Thus, the semiconductor die is subjected to an initial heavy

duty cycle which elicits latent silicon defects. Burn-in testing is usually conducted at elevated potentials and for a prolonged period of time, typically 24 hours, at varying and reduced and elevated temperatures, such as -15°C to 125°C, to accelerate failure mechanisms. Semiconductor dice which survive discrete testing and burn-in are termed "known good die," or ~~"KGD".~~"KGD."

Please replace paragraph number **[0008]** with the following rewritten paragraph:

**[0008]** A common finished semiconductor die package design is a flip-chip design. A ~~flip-chip~~flip-chip semiconductor design comprises a pattern or array of terminations (e.g., bond pads or rerouting trace ends) spaced about an active surface of the semiconductor die for face-down mounting of the semiconductor die to a carrier substrate (such as a printed circuit board, FR4 board, ceramic substrate, or the like). Each termination has a minute solder ball or other conductive connection element disposed thereon for making a connection to a trace end or terminal on the carrier substrate. This arrangement of connection elements is usually referred to as a Ball Grid Array or ~~"BGA".~~ "BGA." The ~~flip-chip~~ flip-chip is attached to the substrate trace ends or terminals, which are arranged in a mirror-image of the BGA, by aligning the BGA thereover and (if solder balls are used) refluxing the solder balls for simultaneous permanent attachment and electrical communication of the semiconductor die to the carrier substrate conductors.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

**[0009]** Such ~~flip-chips~~ flip-chips may be tested and/or burned-in prior to their permanent connection to a carrier substrate by placing each ~~flip-chip~~ flip-chip in a temporary package, such as those discussed above. As shown in FIG. 31, each solder ball 304 attached to a bond pad 302 of a ~~flip-chip~~ flip-chip-configured die 300 is in physical contact with a conductive trace 306 on a contact wall 308 of the temporary package. The conductive traces 306 transmit electrical signals to the die 300 for testing or burn-in. With such a temporary package, each solder ball 304 contacts each conductive trace 306 at only one contact point 310. With only one contact point 310 per ball 304, all of the stresses caused by biasing the die 300 to the contact

wall 308 of the temporary package are concentrated on the one contact point 310 on each solder ball 304. These stresses can result in the solder balls 304 fracturing, dislodging from the bond pad 302, or otherwise damaging the ~~flip-chip~~ flip-chip die 300.

Please replace paragraph number **[0011]** with the following rewritten paragraph:

**[0011]** Therefore, it would be advantageous to develop improved methods and apparatus for use with ~~flip-chip~~ flip-chip-retaining temporary packages, wherein the temporary packages can compensate for irregular solder ball shape and size, and reduce the risk of damage to the semiconductor device under test.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

**[0013]** The interconnections are designed to be formed in a recess, preferably a ~~sloped-wall~~ sloped-wall (either smooth or "stepped") via. Such an interconnection design compensates for undersized or misshapen solder balls on the die under test to prevent a possible false failure indication for the die under test and reduces and reorients the stress on each solder ball when physical contact is made to its mating interconnection.

Please replace paragraph number **[0015]** with the following rewritten paragraph:

**[0015]** The interconnection is preferably circular, as viewed from above, to receive the spherical solder ball, which protrudes partially within the interconnect when placed in contact therewith. Preferably, approximately 10% to 50% of the total height of the solder ball, and preferably about 30% of the total height, will reside within the interconnect. With a spherical solder ball in a smooth ~~sloped-wall~~ sloped-wall via interconnection, each solder ball will make a circular, or at least arcuate, line of contact with the interconnect surface about a periphery of the solder ball, rather than a single contact point. The circular contact distributes the force on the solder ball when the semiconductor substrate is biased against the insert carrying the interconnection in the temporary package, making damage to the solder ball or underlying bond pad less likely. Further, any oxide layer formed on the exterior surface of the solder ball will be

more easily penetrated by the line of contact than through a single contact point effected with prior art interconnections.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

**[0033]** As shown in FIG. 7, a metal layer 120, preferably a metal such as gold, platinum, palladium, tungsten, or the like, to prevent oxidation of the exposed interconnection surface, is applied over the passivation film 106, as well as in the via ~~114~~ 114, by chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), physical vapor deposition (PVD) (sputtering or evaporation), or the like. The metal layer 120 may also be comprised of superimposed metal layers, such as chromium, copper, chromium-copper alloy, titanium, or the like, to effect a better metallurgical connection to conductive trace 104, with a noble metal outer layer for contact with the solder ball.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

**[0038]** As shown in FIG. 23, a metal layer 174 is applied over the passivation film 148, as well as over and into the stepped via 172. A layer of etchant-resistive photoresist film is applied over metal layer 174 and is then masked, exposed, and stripped to form an ~~etchant-resistive~~ etchant-resistive block 176 over the stepped via 172, as shown in FIG. 24. The metal layer 174 surrounding the stepped via 172 is then etched and the etchant-resistive block 176 is stripped to form a discrete interconnection 178, as shown in FIG. 25. The discrete interconnection 178, for example, receives a solder ball 180, which is attached to a bond pad 184 of a semiconductor element 186, such as a die, partial wafer or wafer, as shown in FIG. 26. The discrete interconnection 178 is designed to receive approximately 10% to 50%, and preferably about 30%, of the overall height of the solder ball 180. In other words, the solder ball height segment 188, protruding within the discrete interconnection 178, is approximately 10% to 50%, and preferably about 30%, of the overall height 190 of the solder ball 180.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

**[0041]** The present invention may also be applied to multi-layer conductive trace configurations, as shown in FIG. 29. The multi-layer conductive trace configuration 212 comprises a substrate 214 with a dielectric layer 216 thereof. A lower conductive trace 218 is formed over the dielectric layer 216. A lower passivation layer 220 is formed over the lower conductive trace 218 and the dielectric layer 216. An upper conductive trace 222 is formed on the lower passivation layer 220 and an upper passivation layer 224 is formed over the upper conductive trace 222 and the lower ~~conductive trace 218~~ passivation layer 220. Discrete interconnections 226 and 228 are formed in a manner discussed above to contact the upper conductive trace 222 and the lower conductive trace 218, respectively. The discrete interconnection 228 contacts the lower conductive trace 218 through a conductive column 230 extending through the lower passivation layer 220. It will be understood that such a structure may include three or more trace layers in lieu of the two shown, so as to accommodate a large number of discrete interconnections such as 226 and 228 at a small pitch so as to accommodate one of the aforementioned thousand-plus I/O semiconductor dice.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

**[0042]** FIG. 30 illustrates yet another embodiment of the interconnect of the present invention. Elements common to FIG. 10 and FIG. 30 retain the same numeric designation. The discrete ~~interconnect~~ interconnection 232 is formed by etching the substantially vertical walls for the via rather than sloped walls, but is otherwise formed in a similar method to that described and illustrated in FIGS. 1-9. The discrete interconnection 232 receives a solder ball 126 which is attached to a bond pad 130 of a semiconductor element 128, such as a die or wafer, as shown in FIG. 30. The discrete interconnection 232 is also sized in diameter to receive approximately 10% to 50%, and preferably about 30%, of the overall height of the solder ball 126. In other words, the height 132 received within the discrete interconnection 232 is approximately 10% to 50%, and preferably about 30%, of the overall height 134 of the solder ball 126.

Please replace paragraph number **[0043]** with the following rewritten paragraph:

**[0043]** Although the present disclosure focuses on testing ~~flip-chip~~ flip-chip-configured singulated dice, it is, of course, understood that this technology can be applied on a wafer or partial-wafer scale.

IN THE CLAIMS:

Claims 3-5 have been amended herein. All of the pending claims 1 through 8 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Original) A substrate for testing semiconductor devices, comprising:
a semiconductor substrate having a dielectric layer on an exposed surface thereof;
at least one conductive trace on said dielectric layer;
a passivation layer over said at least one conductive trace and said dielectric layer; and
a metal-lined via in said passivation layer in electrical communication with said at least one conductive trace.

2. (Original) The substrate of claim 1, wherein said metal-lined via is formed of a size and shape to receive approximately 10% to 50% of an overall height of a substantially spherical interconnection element.

3. (Currently Amended) The substrate of claim 2, wherein said metal-lined via is formed of a size and shape to receive approximately 30% of ~~an~~ said overall height of ~~a~~ said substantially spherical interconnection element.

4. (Currently Amended) The substrate of claim 1, wherein said metal-lined via includes sloped sidewalls.

5. (Currently Amended) The substrate of claim 1, wherein said metal-lined via includes stepped sidewalls.

6. (Original) The substrate of claim 1, wherein said at least one conductive trace comprises copper.

7. (Original) The substrate of claim 1, wherein said passivation layer comprises polyimide.

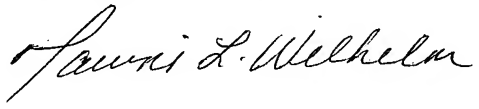
8. (Original) The substrate of claim 1, wherein said metal-lined via comprises a metal from the group comprising gold, platinum, palladium, and tungsten.

## REMARKS

No new matter has been added. The amendments to the claims address typographical and spelling errors, and improve antecedent basis. The amendments do not affect, or surrender, any scope of any claim as originally filed.

The Applicant again requests entry of the amendments as set forth herein prior to examination of the application on the merits.

Respectfully submitted,



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